

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
1875.1040002APPLICATION NO.
(to be assigned) **10/608,013**
(Continuation of U.S. Appl. No. 09/903,502;
Filed: July 13, 2001)APPLICANT
Woo, AgnesFILING DATE
(herewith) **6/30/03**GROUP
(to be assigned) **2838**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
<i>GH</i>	AA1	3,787,717	01/1974	Fischer <i>et al.</i>	317	235 R	12/1971
<i>GH</i>	AB1	4,385,337	05/1983	Asano <i>et al.</i>	361	91	06/1981
<i>GH</i>	AC1	4,423,431	12/1983	Sasaki	357	41	12/1980
<i>GH</i>	AD1	4,763,184	08/1988	Krieger <i>et al.</i>	357	23.13	04/1985
<i>GH</i>	AE1	5,239,440	08/1993	Merrill	361	91	08/1992
<i>GH</i>	AF1	6,437,955	08/2002	Duffy <i>et al.</i>	361	45	03/2000
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
<i>GH</i>	AL1	GB 2 319 893 A	06/1998	Great Britain			Yes No
<i>GH</i>	AM1	WO 00/21134	04/2000	PCT			Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	1	Duvvury <i>et al.</i> , "ESD Protection: Design and Layout Issues for VLSI Circuits," IEEE Transactions on Industry Application, vol. 25 no. 1, January/February 1989, pp. 41-47.
	AS	1	Keller, J. K., "Protection of MOS Integrated Circuits from Destruction by Electrostatic Discharge," IIT Research Institute, 1981, pp. 73-80.
	AT	1	Hulett, T.V., "On Chip Protection of High Density NMOS Devices," pp. 90-96.

EXAMINER **J. Han**DATE CONSIDERED **3/30/04**EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to Applicant.